

## Y/C/RGB/D for NTSC Color TVs

### Description

The CXA2135S is a bipolar IC which integrates the luminance signal processing, chroma signal processing, RGB signal processing, and sync and deflection signal processing functions for NTSC system color TVs onto a signal chip. The IC also includes deflection processing functions for wide TVs.

### Features

- Reduction in peripheral parts  
(ceramic oscillator, AKB sample-and-hold capacitor, etc.)
- I<sup>2</sup>C bus compatible
- Built-in deflection compensation circuit which is capable of supporting various wide modes
- Non-adjusting V oscillator frequency with a countdown system
- Non-interlace display support (even/odd selectable)
- Non-adjusting Y/C filter
- Three sets of CV inputs, two sets of Y/C inputs (can serve as both Y/C and CV inputs), one set of Y/C inputs supports an external combfilter, two sets of RGB inputs, one set of YUV inputs
- It can be outputted YUV on RGB1 inputs
- Built-in dynamic picture and dynamic color circuits
- Built-in AKB and gamma correction circuits
- FSC output

### Applications

Color TVs (4:3, 16:9)

### Structure

Bipolar silicon monolithic IC

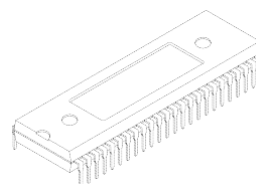
### Absolute Maximum Ratings (Ta = 25°C, GND1, 2 = 0V)

- Supply voltage V<sub>CC1,2</sub> -0.3 to +12 V
- Operating temperature T<sub>opr</sub> -20 to +75 °C
- Storage temperature T<sub>stg</sub> -65 to +150 °C
- Allowable power dissipation P<sub>D</sub> 1.5 W  
(when mounted on a 50mm × 50mm board)
- Voltages at each pin -0.3 to V<sub>CC1,2</sub> + 0.3 V

### Operating Condition

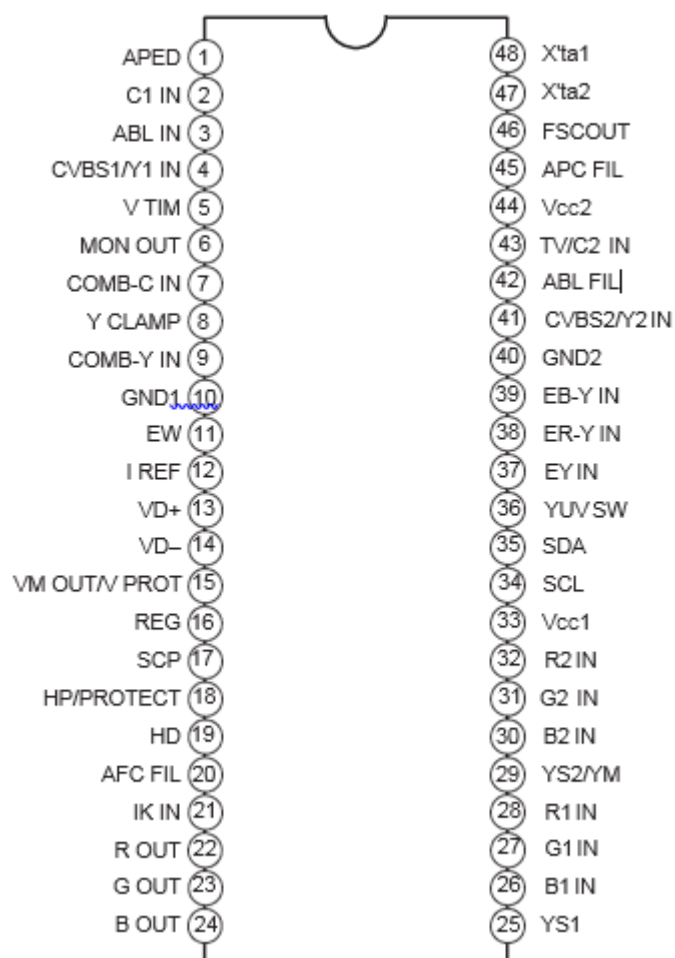
Supply voltage V<sub>CC1,2</sub> 9 ± 0.5 V

48 pin SDIP



Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

## Pin Configuration

PICTURE HARDWARE

## Pin Description

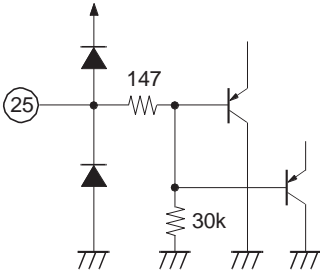
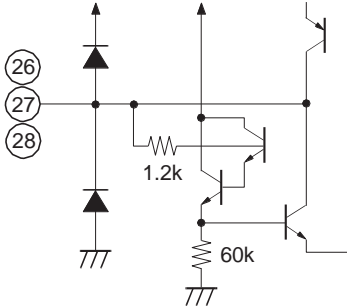
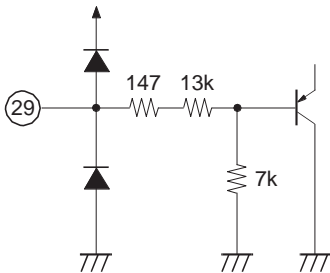
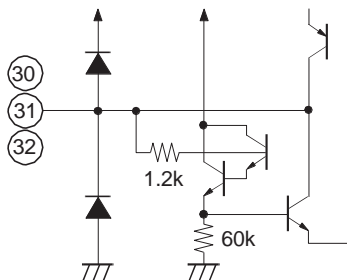
Pin No.	Symbol	Equivalent circuit	Description
1	APED		Capacitor connection for black peak hold of the dynamic picture (black expansion). Connect to GND via a $4.7\mu\text{F}$
2	C1 IN		Chroma signal input. Input a chroma signal with a burst level of 300mVp-p via a $0.1\mu\text{F}$ capacitor. The S terminal signal is normally input.
3	ABL IN		ABL control signal input and VD high voltage fluctuation compensation signal input. High voltage fluctuation compensation has linear control characteristics for the pin voltage range of about 8 to 1V. Control characteristics can be varied through EHT COMP control of the bus. ABL function as PIC/BRT-ABL (average value type). The threshold voltage at which ABL begins to have effect can be switched between 3 to 1V by the bus.
4	CVBS1/Y1 IN		CVBS signal/luminance signal input. Input a 1Vp-p (100% white including sync) CVBS signal via a $1\mu\text{F}$ capacitor. When inputting Y/C separated signal, input the Y signal.

Pin No.	Symbol	Equivalent circuit	Description
5	V TIM		V timing pulse. V timing pulse, HSS and VSS output can be selected by VTIM SEL control of the bus.
6	MON OUT		The signal input from TV, CVBS1 and CVBS2 are selected by VIDEO SEL and S SEL of the bus and output. In the case of S terminal input, the luminance signal and chroma signal are mixed and output. The output level is 2Vp-p including sync.
7	COMB-C IN		Input the chroma signal from the comb filter. Standard input level (burst level) is 0.6Vp-p.
8	Y CLAMP		Capacitor connection for luminance signal clamp. Connect to GND via a 0.1μF capacitor.
9	COMB-Y IN		Input the luminance signal from the comb filter. The signal is input via a 0.1μF capacitor with a level of 2Vp-p. (100% white including sync)

Pin No.	Symbol	Equivalent circuit	Description
10	GND1		GND (the deflection blocks circuit).
11	EW		V parabola wave
12	I REF		Internal reference current setting. Connect to GND via a 10kΩ resistor (metal film resistor) with an error of 1% or less.
13	VD+		V sawtooth wave output. The pin 13 and 14 outputs are the reverse polarity of each other.
14	VD		

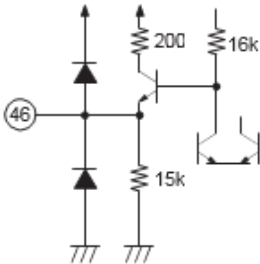
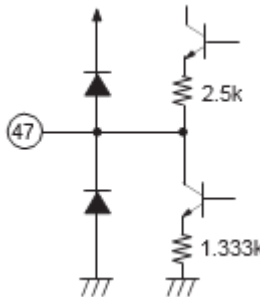
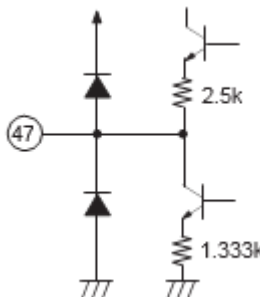
Pin No.	Symbol	Equivalent circuit	Description
15	VM OUT/ V PROT		<p>Output the differential waveform of luminance signal for the VM (Velocity Modulation) system. This pin is also used as the V protect signal input.</p> <p>When a large current (4mA) is pulled from this pin, the RGB outputs are all blanked and "1" is output to the status register VNG.</p>
16	REG		<p>Connect decoupling capacitance for internal regulator. Connect to GND via a 10μF capacitor.</p>
17	SCP		<p>Sand castle pulse output.</p> <p>The sand castle pulse is the waveform obtained by superimposing the burst gate pulse onto the composite blanking pulse.</p>
18	HP/PROTECT		<p>H deflection pulse input for H AFC. Input a 5Vp-p pulse via a capacitor. This pin is also used as the X-RAY protect signal Input. If the pin voltage 1V or less for a 7 vertical cycle or longer, then the hold-down function operates. At this time, the HD output goes to high impedance, the RGB output are blanked and "1" is output to the status register HNG. To release this status, turn the power off and then on again.</p>

Pin No.	Symbol	Equivalent circuit	Description
19	HD		H drive signal output of NPN transistor.
20	AFC FIL		AFC lag-lead filter connection.
21	IK IN		CRT beam current (cathode current IK) input. This current is converted to a voltage inside the IC. This signal is clamped during the V blanking interval to avoid adversely affecting AKB operation for the CRT leak current (max. 100µA). The AKB loop operates by comparing the reference pulse portion of this signal with the Internal reference voltage. The RGB output cutoff can be varied by the bus CUTOFF. The beam current is large during the video interval, so attach a Zener diode of around 4V to this pin to protect the IC.
22 23 24	R OUT G OUT B OUT		R, G and B signal outputs. 2.4Vp-p is outputted during 100% white input. PICTURE: 1Fh DRIVE: 1Fh BRIGHT: 1Fh

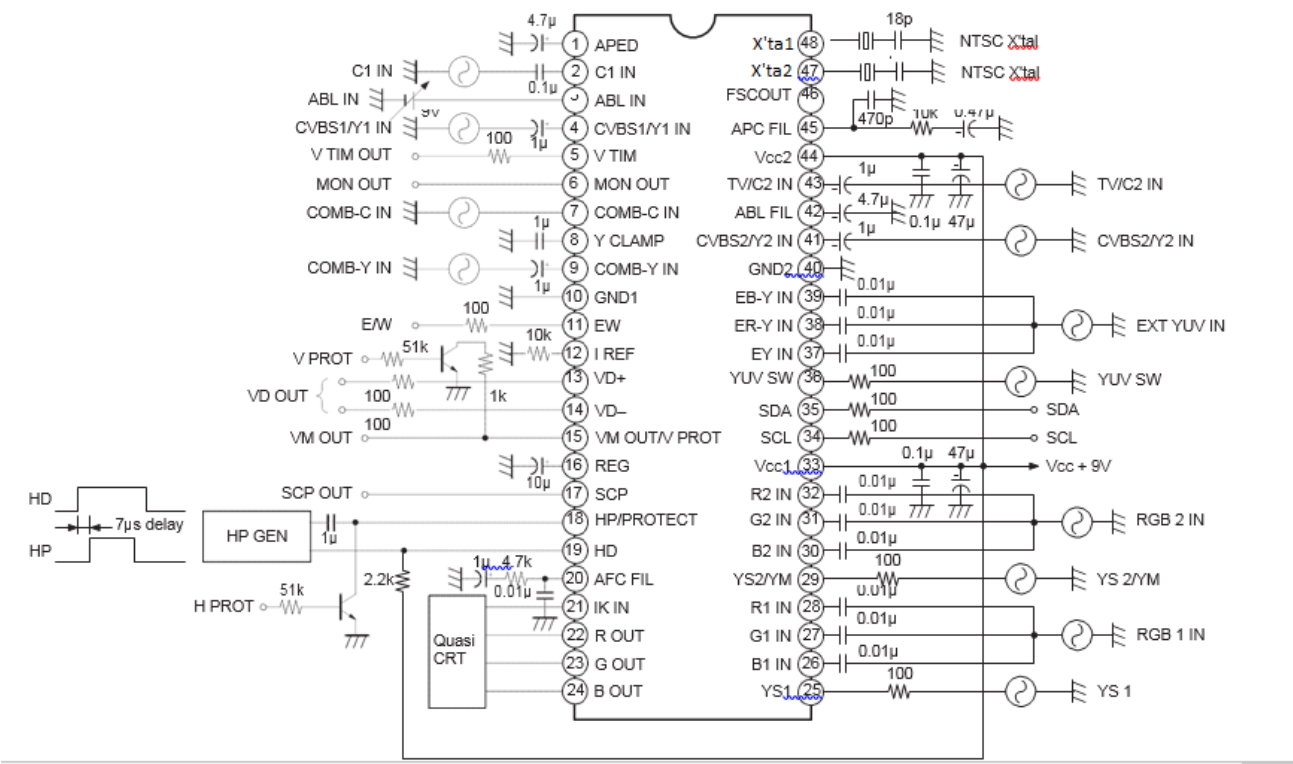
Pin No.	Symbol	Equivalent circuit	Description
25	YS		<p>YS1 switch control. Selects the RGB1 input. YS1 Vth: 0.7V</p> <p>This pin is also used to switch the slave address. When this pin is 7V or more, the slave address changes from 88H to 8AH. SLAVE ADDRESS Vth: 7V</p>
26 27 28	B1 IN G1 IN R1 IN		<p>R1, G1 and B1 signal input. Input a 0.7Vp-p (no sync, 100 IRE) signal via a 0.01μF capacitor. The input signal is clamped at the burst timing in SCP.</p>
29	YS2/YM		<p>YS2/YM switch control. Select the RGB2 input. As YM function, when YM is high (YM Vth: 0.7V), the output signal is attenuated by 10dB. YS2 Vth: 2V</p>
30 31 32	B2 IN G2 IN R2 IN		<p>R2, G2 and B2 signal input. Input a 0.7Vp-p (no sync, 100 IRE) signal via a 0.01μF capacitor. Same as RGB1 IN, the input signal is clamped at the burst timing in SCP. When setting the bus YUV OUT = 1 and connecting 10kΩ resistors to Vcc, Internal YUV signals outputs</p> <ul style="list-style-type: none"> <li>30 Pin: B-Y output</li> <li>31 Pin: R-Y output</li> <li>32 Pin: Y output</li> </ul>
33	Vcc1		Power supply

Pin No.	Symbol	Equivalent circuit	Description
34	SCL		I <sup>2</sup> C Bus protocol SCL (Serial Clock) input.
35	SDA		I <sup>2</sup> C Bus protocol SDA (Serial Data) I/O.
36	YUV SW		YUV SW control. Selects the external YUV input. V <sub>th</sub> : 0.7V This switch has a function prohibited forcibly only the external Y input by the register Y SEL.
37	EY IN		External Y, R-Y and B-Y signal inputs. Input the signal via a 0.01μF capacitor. EY IN: 0.7Vp-p (no sync) ER-Y IN: 0.735Vp-p (75% Color Bar) EB-Y IN: 0.931Vp-p (75% Color Bar)
38 39	ER-Y IN EB-Y IN		

Pin No.	Symbol	Equivalent circuit	Description
40	GND2		GND (for the signal block)
41	CVBS2/Y2 IN		CVBS signal/luminance signal input. Input a 1Vp-p (including sync) signal via a 1 $\mu$ F capacitor. When inputting Y/C separated signals, input the Y signal.
42	ABL FIL		Connect a capacitor (4.7 $\mu$ F) to GND to form the LPF of the ABL control signal.
43	TV/C2 IN		CVBS signal input from the TV tuner or chroma signal input. Input a 1Vp-p (including sync) CVBS signal or a chroma signal with a burst level of 300mVp-p via a 1 $\mu$ F capacitor.
44	Vcc2		Power supply (mainly for the chroma block)
45	APC FIL		Chroma APC lag-lead filter connection.

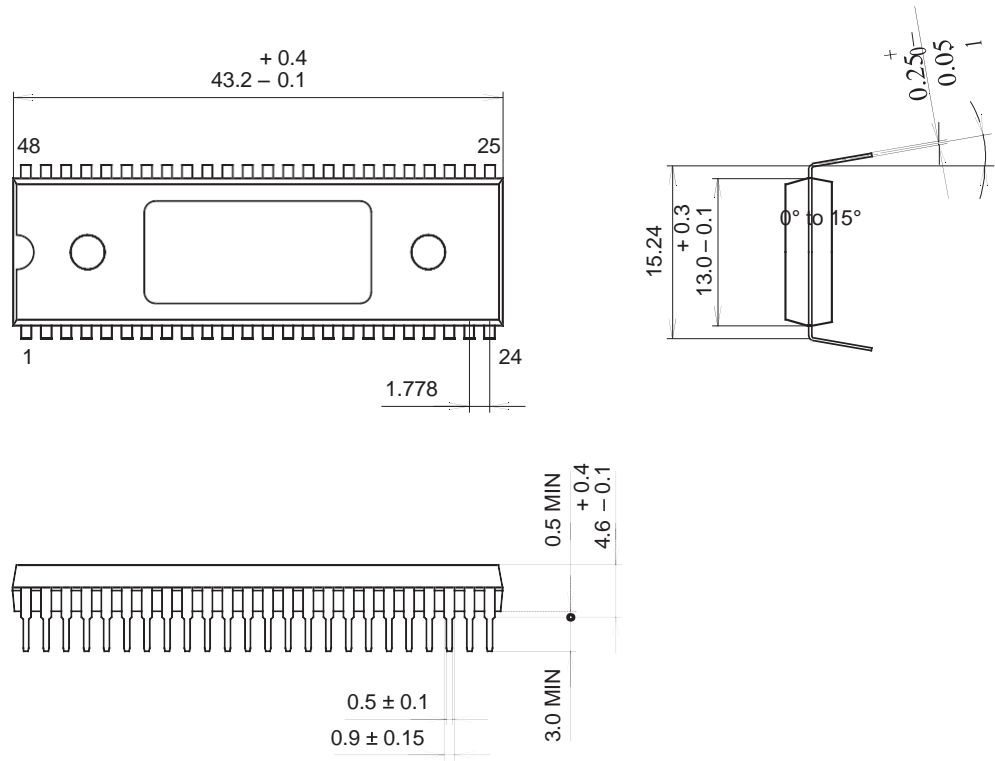
P	Symbol	Equivalent Circuit	Description
46	FSC OUT		FSC output. Output FSC signal by the register FSC SW.
47	X'tal 2		APC crystal connection. X'tal: NTSC crystal (3.579545MHz)
48	X'tal 1		APC crystal connection. X'tal: NTSC crystal (3.579545MHz)

Electrical Characteristic Measurement Circuit



Package Outline      Unit: mm

48PIN SDIP (PLASTIC)



PACKAGE  
STRUCTURE

SONY CODE	SDIP-48P-02
EIAJ CODE	SDIP048-P-0600
JEDEC CODE	—

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	5.1g

NOTE : PALLADIUM PLATING  
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).